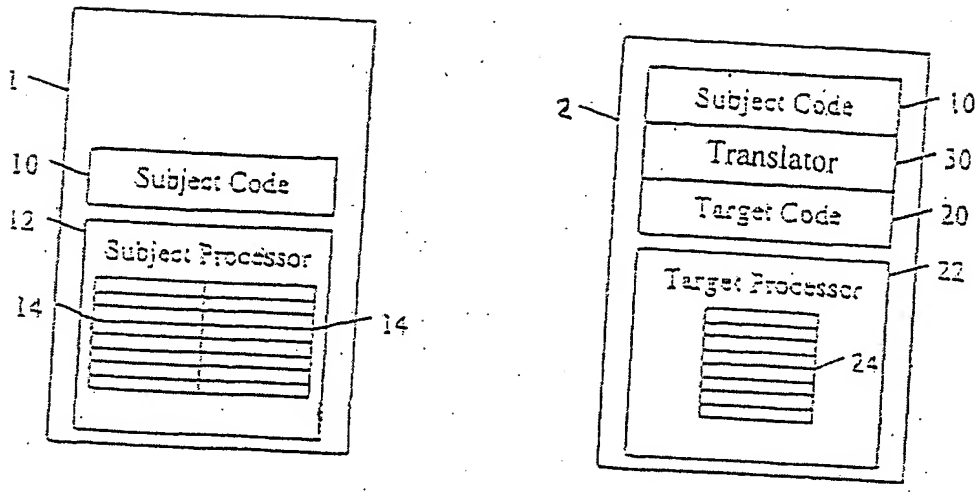

1
10
Subject Code
12
Subject Processor
14
14
2
Subject Code
10
Translator
30
Target Code
20
Target Processor
22
24

FIGURE 1

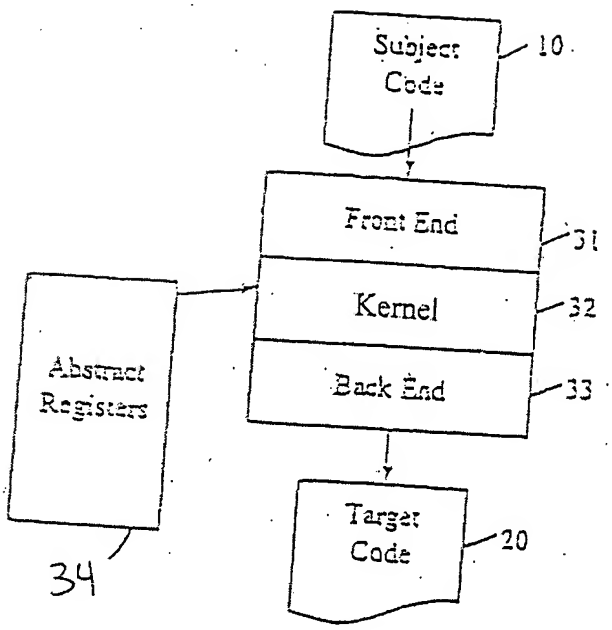

Subject Code
10
Front End
31
Kernel
32
Back End
33
Abstract Registers
34
Target Code
20

FIGURE 2

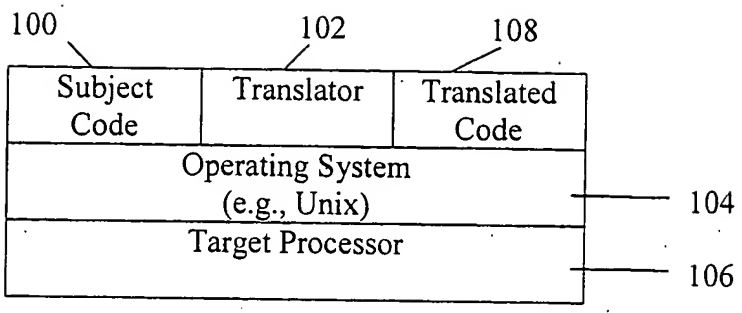

100
102
108
Subject Code
Translator
Translated Code
Operating System (e.g., Unix)
104
Target Processor
106

Figure 3

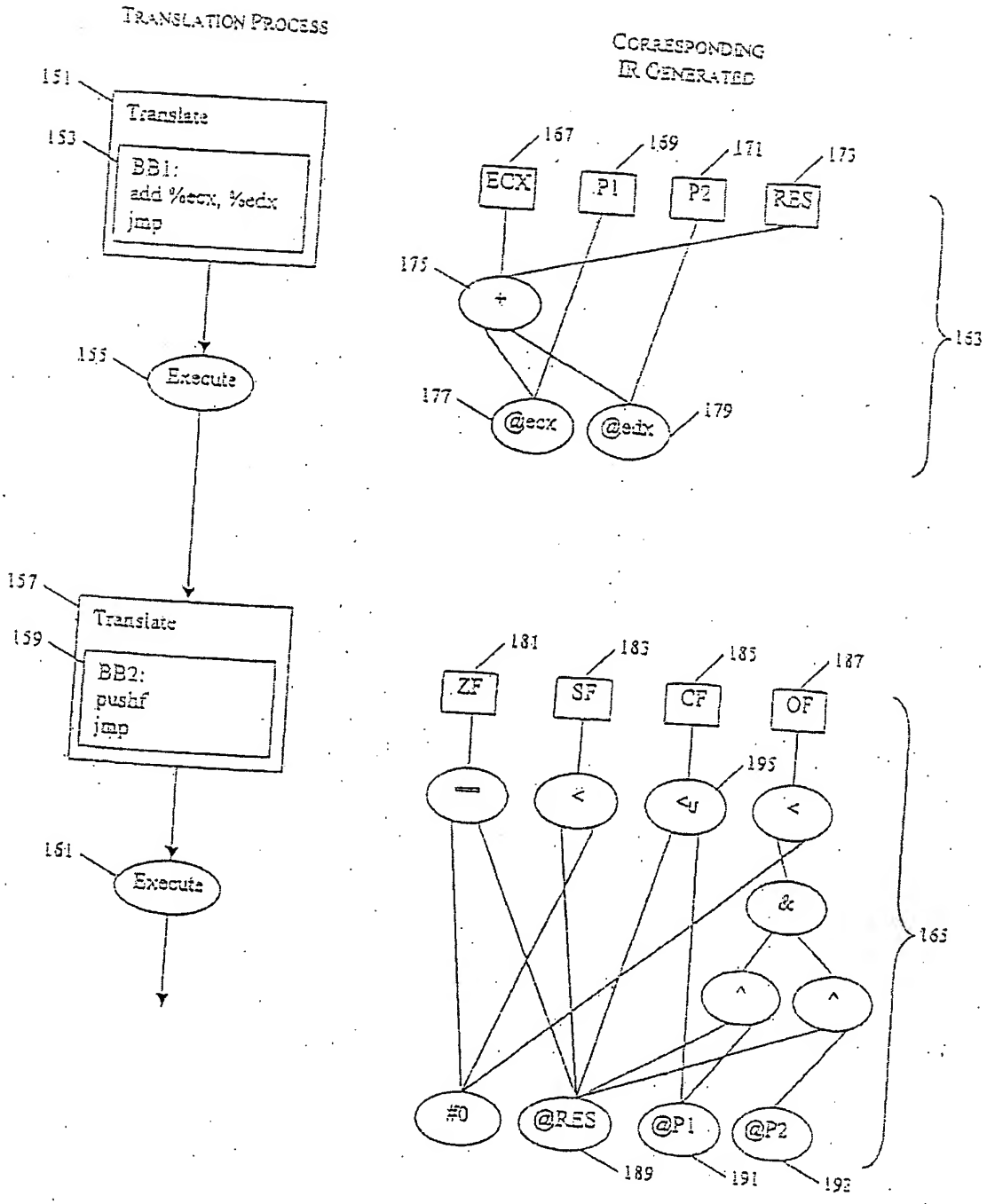

TRANSLATION PROCESS
CORRESPONDING IR GENERATED
151
Translate
153
BB1:
add %ecx, %edx
jmp
155
Execute
157
Translate
159
BB2:
pushf
jmp
161
Execute
167
169
171
173
ECX
P1
P2
RES
175
+
177
@ecx
@edx
179
163
181
183
185
187
ZF
SF
CF
OF
195
—
<
<u
<
&
^
^
#0
@RES
@P1
@P2
189
191
193
165

FIGURE 4

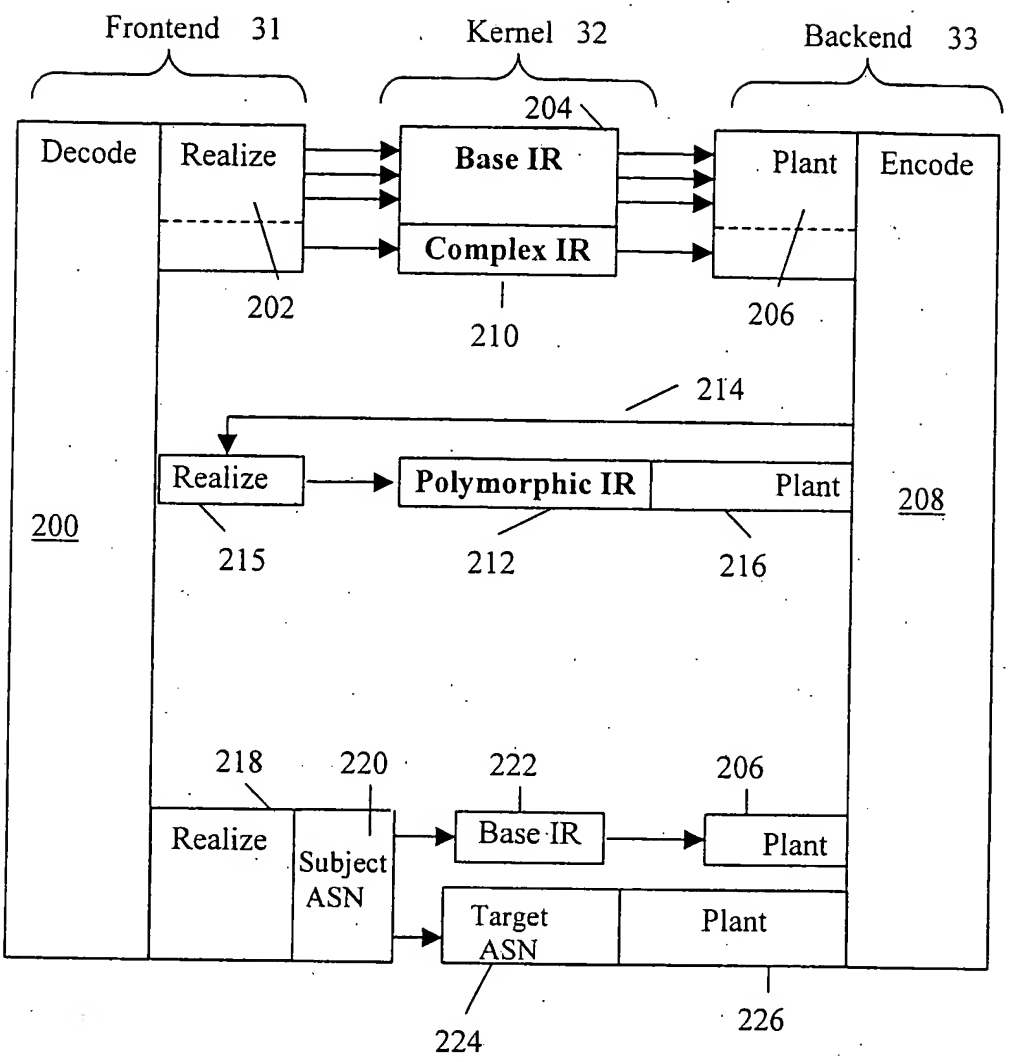
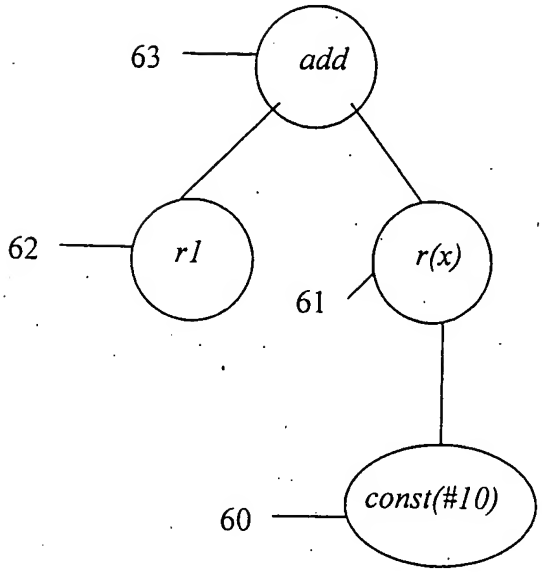

Frontend 31
Kernel 32
Backend 33
204
Decode
Realize
Base IR
Plant
Encode
Complex IR
202
210
206
214
Realize
Polymorphic IR
Plant
200
208
215
212
216
218
220
222
206
Realize
Subject ASN
Base IR
Plant
Target ASN
Plant
224
226

FIG. 5

Instruction: addi r1,#10

Base Node Representation



Complex Node Representation

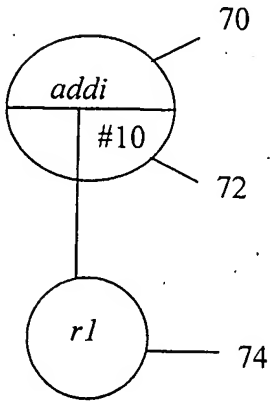


FIG. 6

FIG. 7 MIPS-MIPS ACCELERATOR

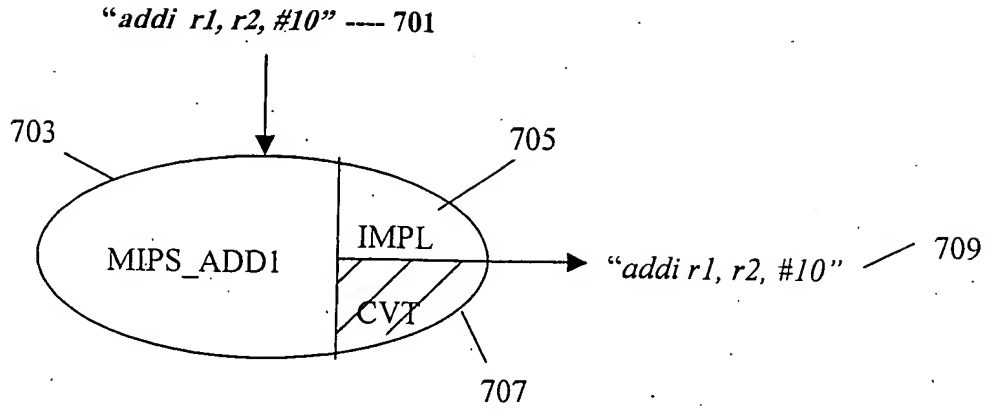


FIG. 8 MIPS-X86 TRANSLATOR

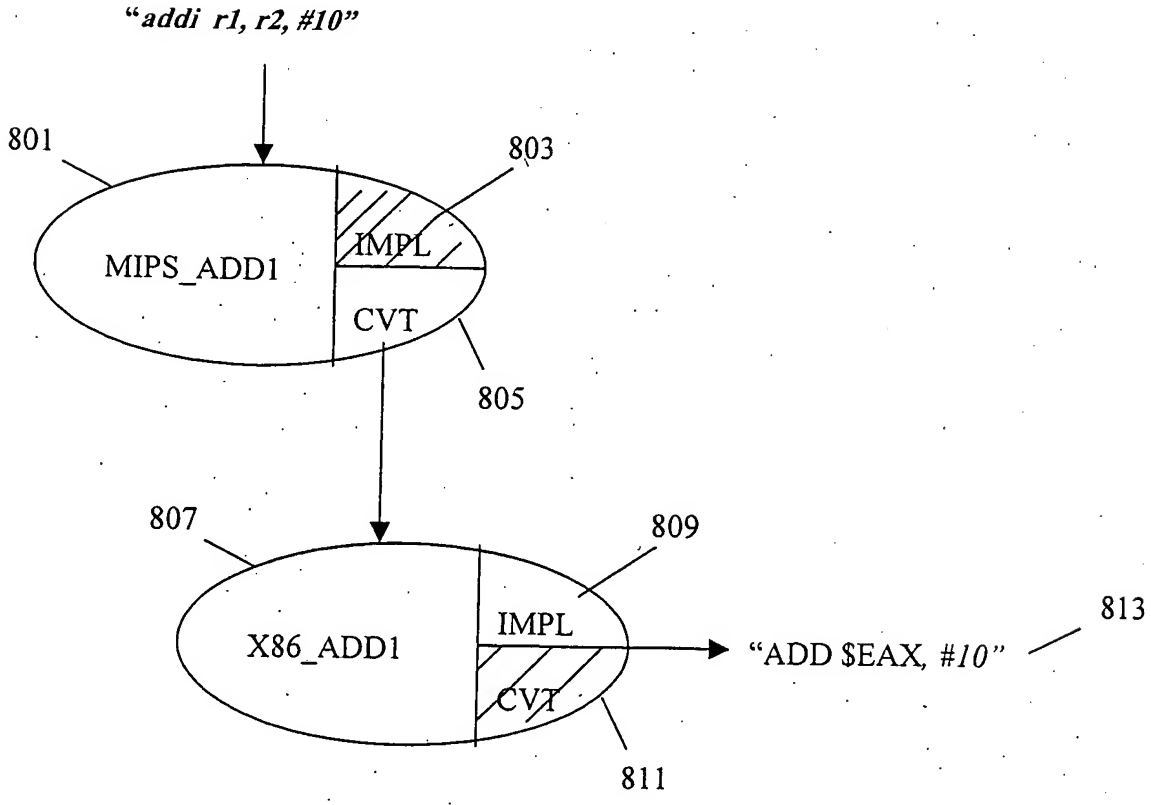
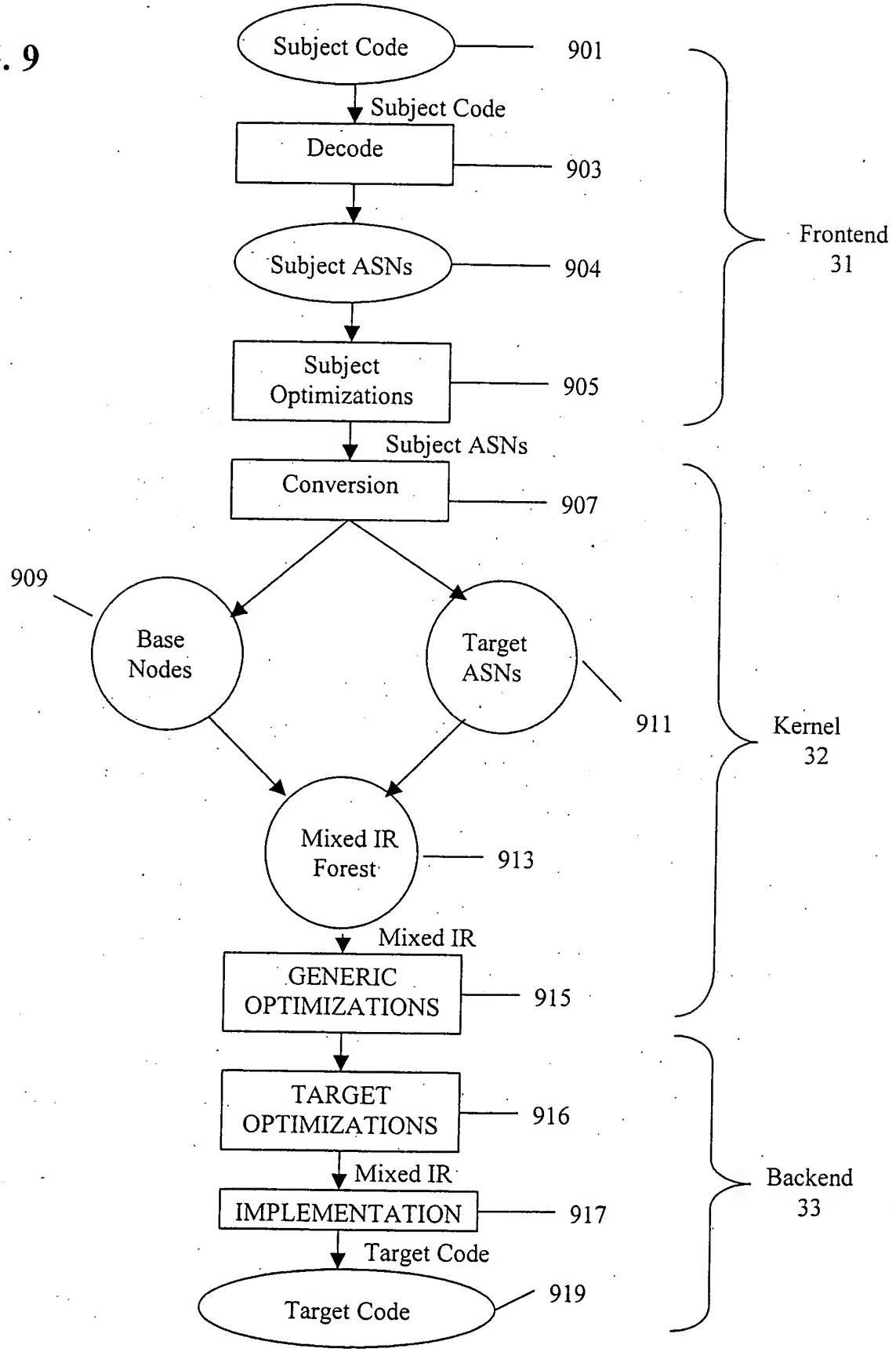


FIG. 9


Subject Code
901
Subject Code
Decode
903
Subject ASNs
904
Subject Optimizations
905
Frontend 31
Subject ASNs
Conversion
907
909
Base Nodes
Target ASNs
911
Kernel 32
Mixed IR Forest
913
Mixed IR
GENERIC OPTIMIZATIONS
915
TARGET OPTIMIZATIONS
916
Mixed IR
IMPLEMENTATION
917
Target Code
Target Code
919
Backend 33

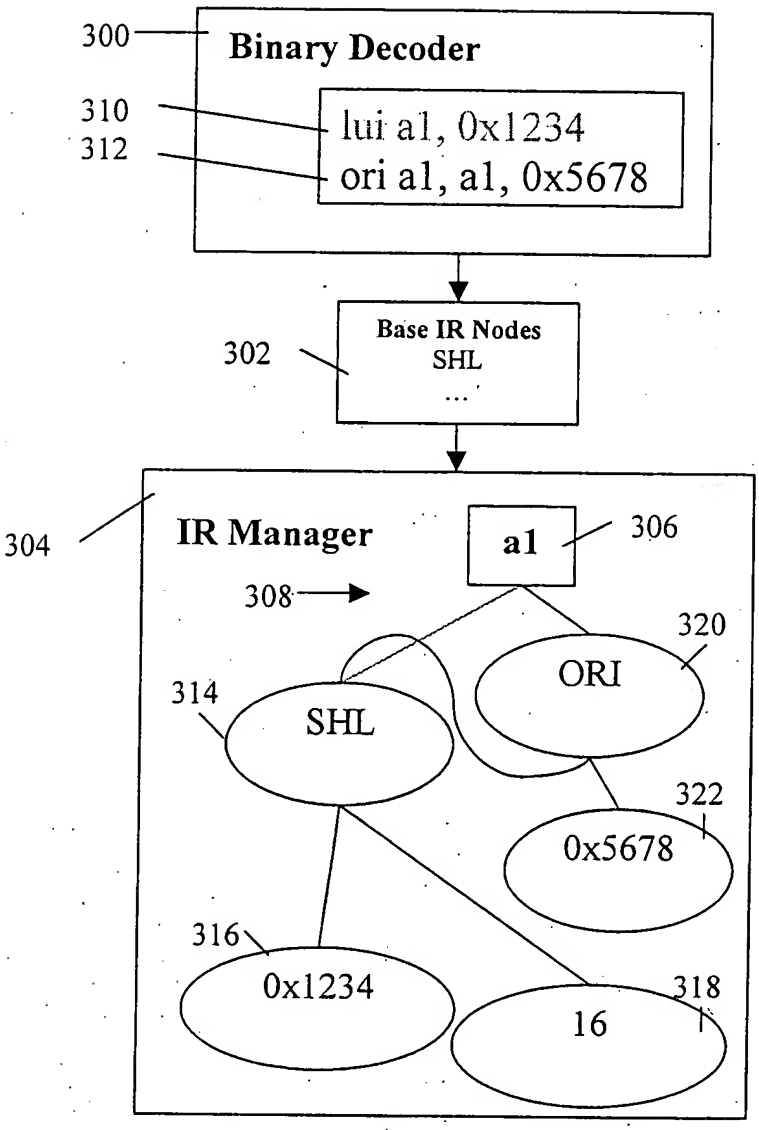

300
Binary Decoder
310
312
lui a1, 0x1234
ori a1, a1, 0x5678
Base IR Nodes
SHL
...
302
304
IR Manager
a1
306
308
320
ORI
314
SHL
322
0x5678
316
0x1234
318
16

FIG. 10

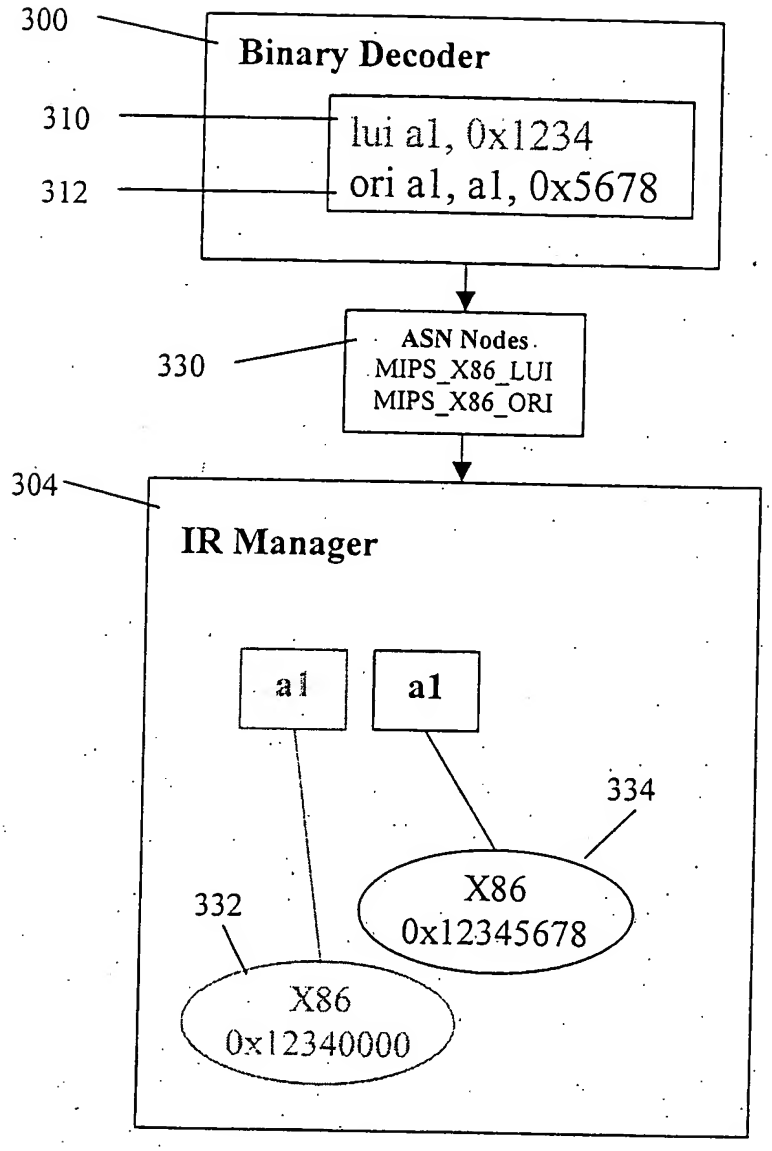

300
Binary Decoder
310
lui a1, 0x1234
312
ori a1, a1, 0x5678
330
ASN Nodes
MIPS_X86_LUI
MIPS_X86_ORI
304
IR Manager
a1
a1
334
X86
0x12345678
332
X86
0x12340000

FIG. 11

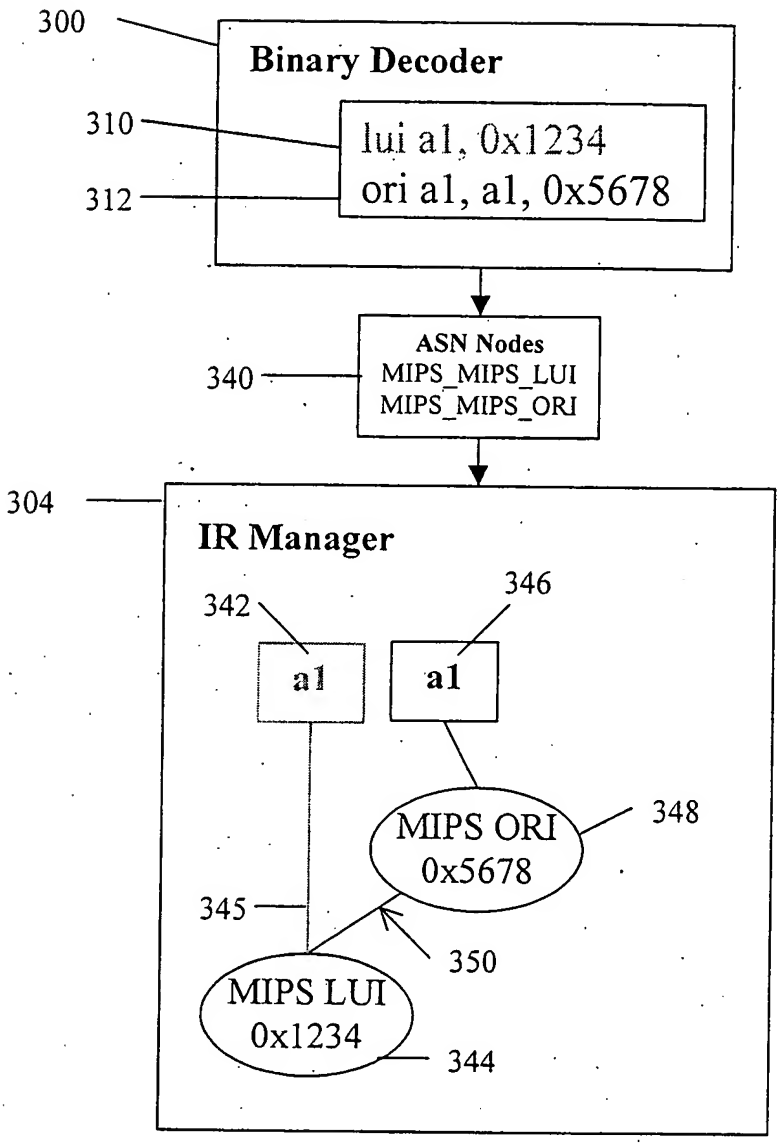

300
Binary Decoder
310
lui a1, 0x1234
312
ori a1, a1, 0x5678
ASN Nodes
340
MIPS_MIPS_LUI
MIPS_MIPS_ORI
304
IR Manager
342
346
a1
a1
MIPS ORI
0x5678
348
345
350
MIPS LUI
0x1234
344

FIG. 12